\*\*\*\*\*\*\*\*\*\*Tutorial 2 tips\*\*\*\*\*\*\*\*\*\*

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***Tip1:***power based on pre place and route netlist and post place and route netlist is different

1. In order to get power report based on pre place and route netlist, need to make some chages:

a. replace all the ‘read -modulename\_routed.v’ with ‘read -modulename\_final.v’ in PAD\_flow.pl



b. In the progress of get SAIF file in the folder SIMULATE, change the command ‘vlog ../../PR/run\_f/moudulname\_routed.v’ to ‘vlog ../../SYNTH/run\_s/modulename\_final.v’

***Tip2:*** Cell power report can help to debug. In order to get cell report, change ‘report’ command in the file PAD\_flow.pl:



***Tip3***: In order to get the correct power report, the period in the command must be the same as the clock period in test fixture.

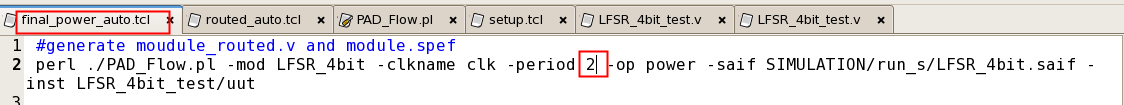
***Tip4***: Simulate circuit in modelsim:

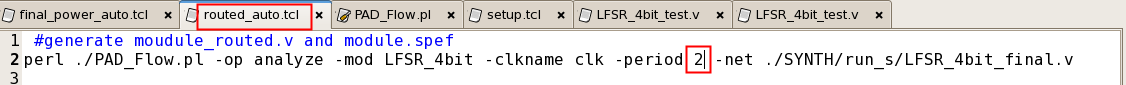
>vlog LFSR.v

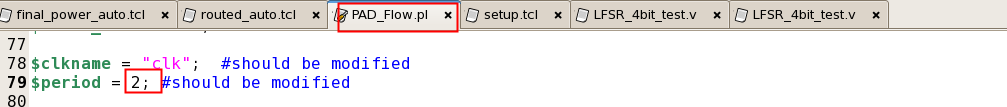
>vlog LFSR\_test.v

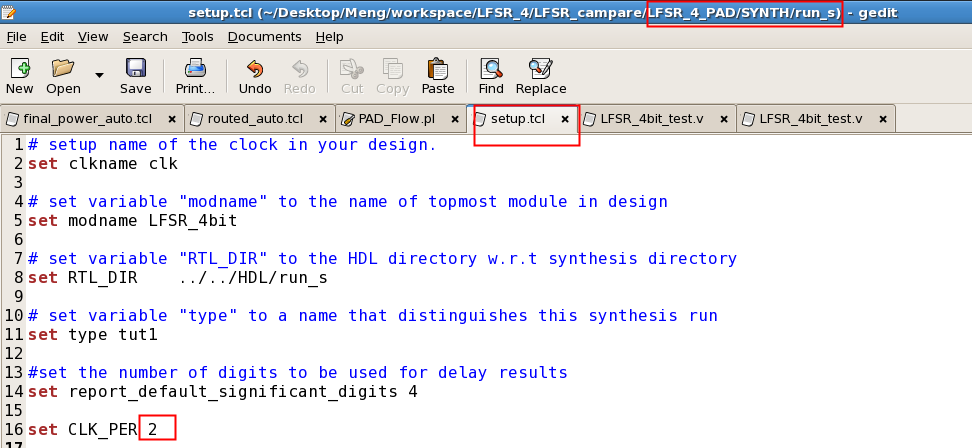
> vsim -voptargs=+acc LFSR\_4bit\_test (is the module name of the test fixture)

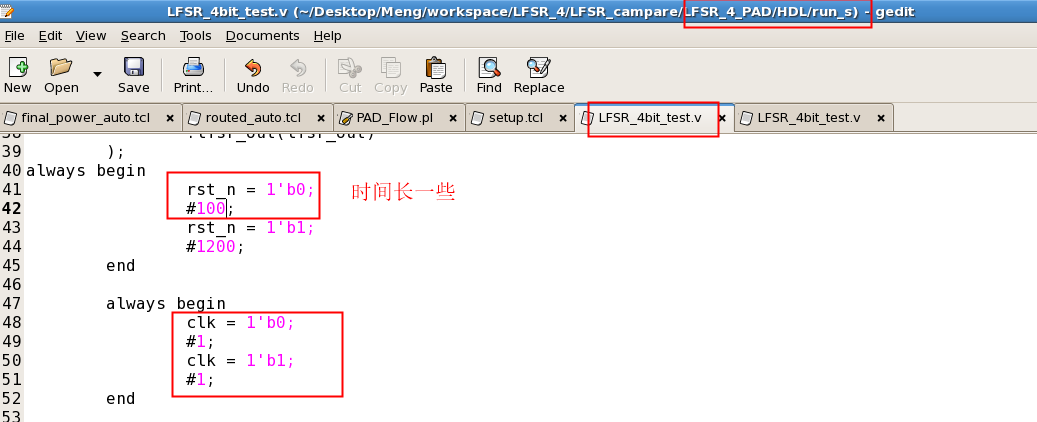
***Tip5***: modify the period in the flow should:

1.

2. 

3. 

4. 

5. 

6. 